Embedded SLC NAND SSD PBGA

FEATURES

- Storage Capacities: 4GB, 8GB, 16GB and 32GB
- Environment conditions:
  - Operating temperature: -40°C to 85°C
  - Storage temperature: -55°C to 125°C
- SLC Flash
- Power consumption
  - 3.3V single power supply
  - Active mode: Read, Write, Erase operation: 120 mA (Typ), 165 mA (Max)
  - Stand by: 2.0 mA (Typ); 3.0 mA (Max)
- Interface modes
  - ATA-6 compatible in True IDE mode
- Less than 1 Error in 10^{14} bits read
- MTBF > TBD
- High shock & vibration tolerance
- W/E Endurance: TBD
- High performance
  - Interface Transfer speed in PIO mode 6
  - Typical write: 30 MBytes/s in ATA PIO mode 6
  - Typical read: 45 MBytes/s in ATA PIO mode 6
  - On card ECC up to 4 Bytes per 512 Byte data sector
- Dimensions:
  - (27mm x 22mm x 3.55mm) Max (before soldering)
- Highly resistant to data corruption due to power loss
- Single device connector free solution for embedded environments
- Sophisticated wear leveling firmware
- Enhanced reliability with a 1.27mm pitch; eutectic tin-lead solder ball

DESCRIPTION

The W7NxVHxxBI is a small reliable solid state storage solution in a single integrated BGA package. Typical NAND related concerns like proper wear leveling, sufficient error correction, as well as power interruption protection is managed by the integrated 32-bit RISC flash controller. Consuming extremely little power while providing high performing data rates makes this solution an attractive storage alternative for embedded products. The PBGA is easy to integrate and will consume very little battery life when compared to hard drives and other larger form factor SSD solutions.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

TABLE 1

Item	Size	Performance
W7N4GVHxxBI	4GB	3.0 to 3.60
W7N8GVHxxBI	8GB	3.0 to 3.60
W7N16GVHxxBI	16GB	3.0 to 3.60
W7N32GVHxxBI	32GB	3.0 to 3.60

DENSITY COMPARISONS

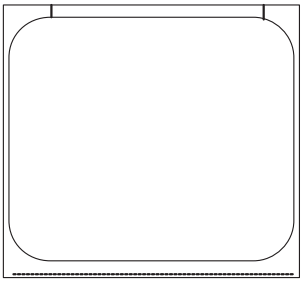
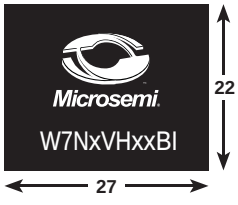
	Standard CF Card	W7NxVHxxBI	SAVINGS
			
Area	**1558mm²**	**594mm²**	**63%**

FIGURE 1 – 224 PBGA PIN CONFIGURATION – TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A		NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
C	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	GND	GND	IOCS16# (IOIS16#) (WP)	IORDY (WAIT#)	DMACK# (REG#)	CSEL#	PDIAG# (STSCHG#) (BVD1)	GND	GND	NC	NC	NC
E	NC	NC	NC	GND	DASP# (SPKR#) (BVD2)	DMARQ (INPACK#)	WE#	CS1# (CE2#)	CS0# (CE1#)	IORD#	D00	GND	NC	NC	NC
F	NC	NC	NC	V_{CC}	NC	INTRQ (IREQ#) (READY)	IOWR#	ATASEL# (OE#)	D08	D14	D09	D10	NC	NC	NC
G	NC	NC	NC	V_{CC}	V_{CC}	NC	GND	GND	GND	GND	D01	D15	NC	NC	NC
H	NC	NC	NC	V_{CC}	NC	NC	GND	GND	GND	D07	D04	V_{CC}	NC	NC	NC
J	NC	NC	NC	RESET# (RESET)	NC	GND	GND	GND	V_{CC}	D12	V_{CC}	V_{CC}	NC	NC	NC
K	NC	NC	NC	NC	A03	A02	A05	A10	D05	D03	D11	V_{CC}	NC	NC	NC
L	NC	NC	NC	GND	A00	A01	A06	A09	D06	D13	DNU	GND	NC	NC	NC
M	NC	NC	NC	GND	GND	A04	A07	A08	DNU	D02	GND	GND	NC	NC	NC
N	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
P	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
R	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

ENVIRONMENTAL CHARACTERIZATION

Item	Performance
Temperature Cycle	JEDEC - JESD STD A104 Temp condition N (-40°C to 85 °C) and soak mode 3; 200 cycles
Humidity	MIL-STD 810F, Method 507.4, Paragraph 4.5.2 - 10 day test per figure 507.4-1, 10 day test
Vibration	MIL-STD 810F, Method 514.5, procedure 1, category 24, 1 hour per axis
Shock	MIL-STD 810F, Method 516.5, procedure1, non-operational, 40g, SRS functional shock for ground equipment, three (3) shock per axis (positive or negative). JEDEC- JESD22-B, 104-A, test condition B,1500 g pulse, 0.5 msec
Altitude	MIL-STD 810F, Method 500.4, procedure II, modified to 80,000 ft and non operation 1 hr test duration at altitude

PRODUCT RELIABILITY

Item	Value
MTBF (@ 25°C)	TBD
Data reliability	< 1 Non-Recoverable Error in 10^{14} Bits Read
Endurance	TBD

PRODUCT PERFORMANCE

Item	Performance (PIO mode 6 true IDE)	UDMA Mode 4	MDMA Mode 4
Read Transfer Rate (Typical)	45MB/s	TBD	TBD
Write Transfer Rate (Typical)	30MB/s	TBD	TBD
Controller Overhead (Command to DRQ)	1ms typical, 5ms (max)	TBD	TBD

Note: 1. Conditions for performance measured TBD.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Free-Air Temperature	T_A	-40	+85	C
Storage Temperature	T_{STG}	-40	+105	C
Signal Voltage Relative to GND	V_G	-0.5	V_{CC} +0.5	V
Supply Voltage	V_{CC}	-0.5	4.0	V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Supply Voltage Range	3.0	3.6	V	
V_{IL}	Input LOW Voltage	-0.3	+0.8	V	—
V_{IH}	Input HIGH Voltage	2.0	VCC+0.3	V	—
V_{OL}	Output LOW Voltage	—	0.45	V	at 4mA
V_{OH}	Output HIGH Voltage	2.4		V	-1mA
I_{CC}	Operating Current, V_{CC} = 3.3V				
	Sleep Mode	—	0.55	mA	—
	Operating	—	165	mA	—
I_{LI}	Input Leakage Current	—	±10	µA	—
I_{LO}	Output Leakage Current	—	±10	µA	—
$C_{I,O}$	Input/Output Capacitance	—	10	pF	—

ATTRIBUTE MEMORY READ AND WRITE AC CHARACTERISTICS

3.3 V ±0.3V

Symbol	Parameter	Min	Max	Units
t_{cR}	Read Cycle Time	250	—	ns
$t_{a(A)}$	Address Access Time	—	250	ns
$t_{a(CE)}$	Card Enable Access Time	—	250	ns
$t_{a(OE)}$	Output Enable Access Time	—	125	ns
$t_{dis(CE)}$	Output Disable time from CE#	—	100	ns
$t_{dis(OE)}$	Output Disable time from OE#	—	100	ns
$t_{en(CE)}$	Output Enable time from CE#	5	—	ns
$t_{en(OE)}$	Output Enable time from OE#	5	—	ns
$t_{v(A)}$	Data valid time from address change	0	—	ns
$t_{su(A)}$	Address Setup Time	30	—	ns
$t_{h(A)}$	Address Hold Time	20	—	ns
$t_{su(CE)}$	Card Enable Setup Time	0	—	ns
$t_{h(CE)}$	Card Enable Hold Time	20	—	ns
t_{cW}	Write Cycle Time	250	—	ns
$t_{w(WE)}$	Write Pulse TIme	150	—	ns
$t_{su(A-WEH)}$	Address setup time for WE#	30	—	ns
$t_{su(CE-WEH)}$	Card Enable setup time for WE#	30	—	ns
$t_{su(D-WEH)}$	Data setup time for WE#	80	—	ns
$t_{h(D)}$	Data hold time	30	—	ns
$t_{dis(WE)}$	Output disable time from WE#	—	100	ns
$t_{en(WE)}$	Output enable time from WE#	5	—	ns
$t_{su(OE-WE)}$	Output Enable setup time for WE#	10	—	ns
$t_{h(OE-WE)}$	Output Enable hold time from WE#	10	—	ns

COMMON MEMORY READ AND WRITE AC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
t_{cR}	Read Cycle Time	80	—	ns
$t_{a(A)}$	Address Access Time	—	55	ns
$t_{a(CE)}$	Card Enable Access Time	—	55	ns
$t_{a(OE)}$	Output Enable Access Time	—	45	ns
$t_{dis(CE)}$	Output Disable time from CE#	—	45	ns
$t_{dis(OE)}$	Output Disable time from OE#	—	45	ns
$t_{en(CE)}$	Output Enable time from CE#	5	—	ns
$t_{en(OE)}$	Output Enable time from OE#	5	—	ns
$t_{V(A)}$	Data valid time from address change	0	—	ns
$t_{su(A)}$	Address Setup Time	10	—	ns
$t_{h(A)}$	Address Hold Time	10	—	ns
$t_{su(CE)}$	Card Enable Setup Time	0	—	ns
$t_{h(CE)}$	Card Enable Hold Time	10	—	ns
t_{cW}	Write Cycle Time	80	—	ns
$t_{w(WE)}$	Write Pulse TIme	55	—	ns
$t_{su(A-WEH)}$	Address setup time for WE#	10	—	ns
$t_{su(CE-WEH)}$	Card Enable setup time for WE#	0	—	ns
$t_{su(D-WEH)}$	Data setup time for WE#	30	—	ns
$t_{h(D)}$	Data hold time	10	—	ns
$t_{rec(WE)}$	Data record time from WE#	15	—	—
$t_{dis(WE)}$	Output disable time from WE#	—	45	ns
$t_{en(WE)}$	Output enable time from WE#	5	—	ns
$t_{su(OE-WE)}$	Output Enable setup time for WE#	10	—	ns
$t_{h(OE-WE)}$	Output Enable hold time from WE#	10	—	ns

I/O ACCESS READ AND WRITE AC CHARACTERISTIC

Symbol	Parameter	Min	Max	Units
$t_{d(IORD)}$	Data Delay after IORD#	—	45	ns
$t_{h(IORD)}$	Data Hold following IORD#	5	—	ns
$t_{w(IORD)}$	IORD# pulse width	55	—	ns
$t_{suA(IORD)}$	Address setup time for IORD#	15	—	ns
$t_{hA(IORD)}$	Address hold time for IORD#	10	—	ns
$t_{suCE(IORD)}$	Card Enable setup time for IORD#	5	—	ns
$t_{hCE(IORD)}$	Card Enable hold time from IORD#	10	—	ns
$t_{suREG(IORD)}$	REG setup time for IORD#	5	—	ns
$t_{hREG(IORD)}$	REG Hold time from IORD#	0	—	ns
$t_{dfINP(IORD)}$	INPACK delay falling from IORD#	0	45	ns
$t_{drINP(IORD)}$	INPACK delay rising from IORD#	—	45	ns
$t_{dfIO16(IORD)}$	IOIS16 delay falling from address	—	35	ns
$t_{drIO16(IORD)}$	IOIS16 delay rising from address	—	35	ns
$t_{su(IOWR)}$	Data setup time for IOWR#	15	—	ns
$t_{h(IOWR)}$	Data hold time from IOWR#	5	—	ns
$t_{w(IOWR)}$	IOWR# pulse width	55	—	ns
$t_{suA(IOWR)}$	Address setup time for IOWR#	15	—	ns
$t_{hA(IOWR)}$	Address hold time from IOWR#	10	—	ns
$t_{suCE(IOWR)}$	Card Enable setup time for IOWR#	5	—	ns
$t_{hCE(IOWR)}$	Card Enable hold time from IOWR#	10	—	ns
$t_{suREG(IOWR)}$	REG setup time for IOWR#	5	—	ns
$t_{hREG(IOWR)}$	REG hold tme from IOWR#	0	—	ns

TRUE-IDE PIO MODE READ AND WRITE CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
t_0	Cycle time	80	—	ns
t_1	Address setup time for IORD#/IOWR#	10	—	ns
t_9	Address hold time from IORD#/IOWR#	10	—	ns
t_2	IORD#/IOWR# pulse width	55	—	ns
t_{2i}	IORD#/IOWR# recovery time	20	—	ns
t_5	Data setup time for IORD#	10	—	ns
t_6	Data setup time for IORD#	5	—	ns
t_{6Z}	Output disable time from IORD#	—	20	ns
t_3	Data setup time for IOWR#	15	—	ns
t_4	Data hold following IOWR#	5	—	ns

TRUE-IDE MDMA MODE READ AND WRITE CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
t_O	Cycle time	80	—	ns
t_D	IORD#/IOWR# pulse width	55	—	ns
t_E	IORD# data access	—	45	ns
t_F	Data hold following IORD#	5	—	ns
t_G	Data setup time for IORD#/IOWR#	10	—	ns
t_H	Data hold following IOWR#	5	—	ns
t_I	DMACK# setup time for IORD#/IOWR#	0	—	ns
t_J	DMACK# hold following IORD#/IOWR#	5	—	ns
t_{KR}, t_{KW}	IORD#/IOWR# recovery time	20	—	ns
t_{LR}, t_{LW}	IORD#/IOWR# to DMARQ delay	—	35	ns
t_M	CS0#, CS1# setup for IORD#/IOWR#	5	—	ns
t_N	CS0#, CS1# hold following IORD#/IOWR#	10	—	ns
t_Z	Output disable time from DMACK#	—	25	ns

TRUE-IDE IDMA MODE READ AND WRITE CHARACTERISTICS

The interface timing in the True-IDE UDMA modes is not only depending on the interface hardware, but also on the correct setup of the UDMA registers in the firmware, according to the UDMA transfer mode selected by the host. With a correct register setup, the interface timing complies to the UDMA Mode 0 to Mode 4 timing specifications of the CF Specification Revision 4.1, and to the UDMA Mode 0 to Mode 4 timing specifications of the ATA/ATAPI-6 Standard.

PIN ASSIGNMENTS & PIN TYPE

TBD		
Pin Number	Signal Name	Pin Type
A02-A15	NC	No Connect
B01-B15	NC	No Connect
C01-C15	NC	No Connect
D01-D03	NC	No Connect
D04	GND	Ground
D05	GND	Ground
D06	IOCS16# (IOIS16#) (WP)	O
D07	IORDY (WAIT#)	O
D08	DMACK# (REG#)	I
D09	CSEL#	I
D10	PDIAG# (STSCHG#) (BVD1)	I/O
D11	GND	Ground
D12	GND	Ground
D13-D15	NC	No Connect
E01-E03	NC	No Connect
E04	GND	Ground
E05	DASP# (SPKR#) (BVD2)	I/O
E06	DMARQ (INPACK#)	O
E07	WE#	I
E08	CS1# (CE2#)	I
E09	CS0# (CE1#)	I
E10	IORD#	I
E11	D00	I/O
E12	GND	Ground
E13-E15	NC	No Connect
F01-F03	NC	No Connect
F04	V_{CC}	Power
F05	NC	No Connect
F06	INTRQ (IREQ#) (READY)	O
F07	IOWR#	I
F08	ATASEL# (OE#)	I
F09	D08	I/O
F10	D14	I/O
F11	D09	I/O
F12	D10	I/O
F13-F15	NC	No Connect
G01-G03	NC	No Connect
G04	V_{CC}	Power
G05	V_{CC}	Power
G06	NC	No Connect
G07	GND	Ground
G08	GND	Ground
G09	GND	Ground
G10	GND	Ground
G11	D01	I/O
G12	D15	I/O
G13-G15	NC	No Connect
H01-H03	NC	No Connect
H04	V_{CC}	Power
H05	NC	No Connect
H06	NC	No Connect
H07	GND	Ground

TBD		
Pin Number	Signal Name	Pin Type
H08	GND	Ground
H09	GND	Ground
H10	D07	I/O
H11	D04	I/O
H12	VCC	Power
H13-H15	NC	No Connect
J01-J03	NC	No Connect
J04	RESET# (RESET)	I
J05	NC	No Connect
J06	GND	Ground
J07	GND	Ground
J08	GND	Ground
J09	V_{CC}	Power
J10	D12	I/O
J11	V_{CC}	Power
J12	V_{CC}	Power
J13-J15	NC	No Connect
K01-K03	NC	No Connect
K04	NC	No Connect
K05	A03	I
K06	A02	I
K07	A05	I
K08	A10	I
K09	D05	I/O
K10	D03	I/O
K11	D11	I/O
K12	V_{CC}	Power
K13-K15	NC	No Connect
L01-L03	NC	No Connect
L04	GND	Ground
L05	A00	I
L06	A01	I
L07	A06	I
L08	A09	I
L09	D06	I/O
L10	D13	I/O
L11	DNU	Do Not Use
L12	GND	Ground
L13-L15	NC	No Connect
M01-M03	NC	No Connect
M04	GND	Ground
M05	GND	Ground
M06	A04	I
M07	A07	I
M08	A08	I
M09	DNU	Do Not Use
M10	D02	I/O
M11	GND	Ground
M12	GND	Ground
M13-M15	NC	No Connect
N01-N15	NC	No Connect
P01-P15	NC	No Connect
R01-R15	NC	No Connect

SIGNAL DESCRIPTION

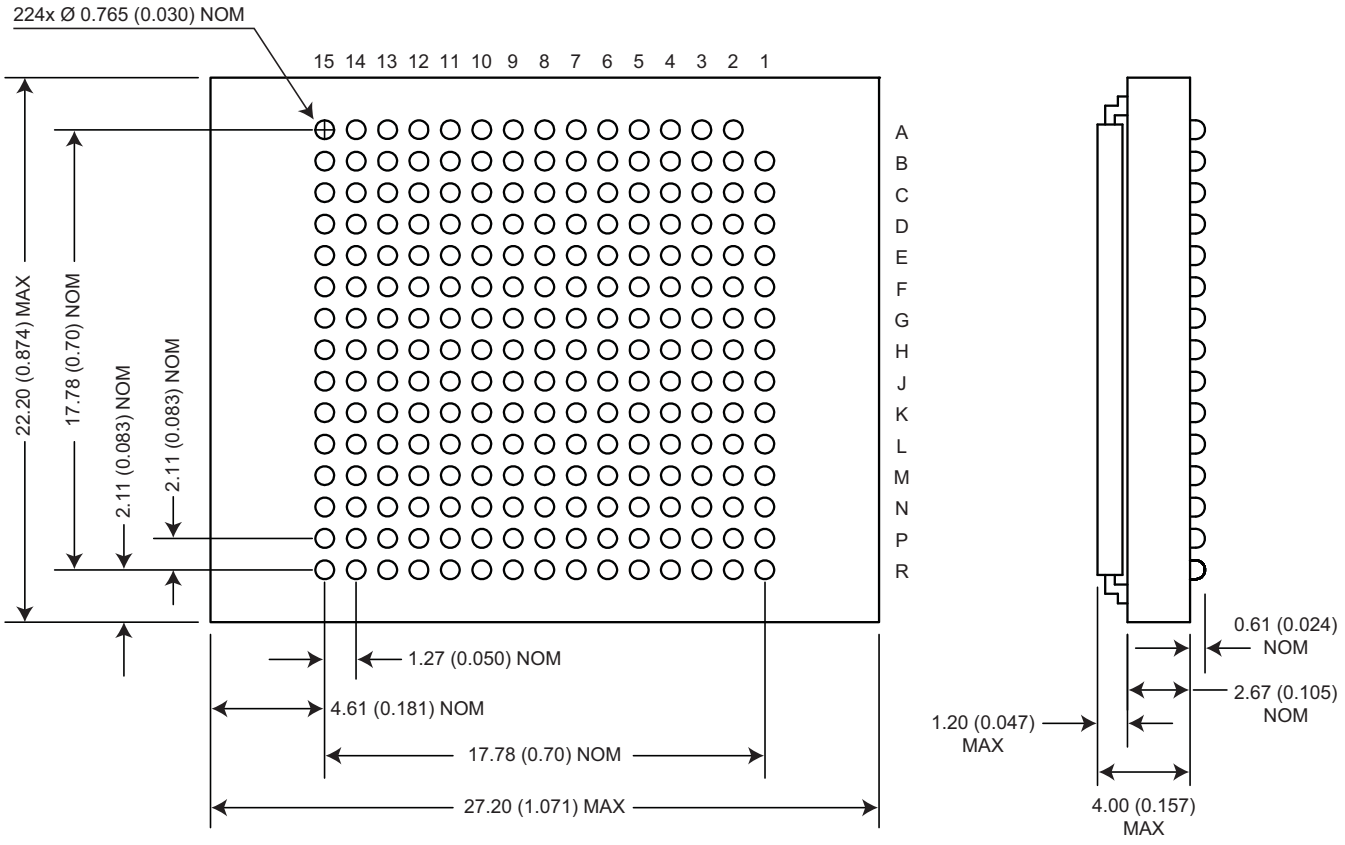
Signal Name	Dir.	Description
CS0# (CE1#)	I,U	Card Enable 1
CS1# (CE2#)		Card Enable 2
DMACK# (REG#)	I	DMA Acknowledge (Attribute Memory or I/O Enable)
WE#	I,U	Memory Write Enable
ATASEL# (OE#)		True-IDE Mode select (Output Enable)
IOWR# (STOP)		I/O Write Enable (Terminate ultra DMA data burst)
IORD#		I/O Read Enable
CSEL#		True-IDE Master/Slave select
RESET# (RESET)		Reset signal. This pin includes an input fi lter that fi lters pulses shorter than about 40 ns.
A10..A00	I/O	Address Bus. Unused pins may be left open, or connected to GND.
D15..D00		Data Bus
DMARQ (INPACK#)	O,U	DMA Acknowledge (Input Acknowledge)
INTRQ (IREQ#) (READY)		Interrupt Request (Interrupt Request) (Ready/Busy signal)
PDIAG# (STSCHG#) (BVDI)		True-IDE DIAG (Status Change) (Unsupported)
DASP# (SPKR#)(BVD2)	I/O,U	True-IDE DASP (Unsupported) (Unsupported)
IORDY (WAIT#)		I/O Ready (UDMA DDMARDY#, DSTROBE) (Wait)
IOCS16# (IOIS16#) (WP)	O	Word Data Transfer (I/O is 16 bit signal) (Write Protect)

TYPICAL SERIES TERMINATION FOR ULTRA DMA

Signal	Host Termination	Device Termination
IORD# (HDMARDY#, HSTROBE)	22 ohm	82 ohm
IOWR# (STOP)	22 ohm	82 ohm
CS0#, CS1#	33 ohm	82 ohm
A00, A01, A02	33 ohm	82 ohm
DMACK#	22 ohm	82 ohm
D00 through D15	33 ohm	33 ohm
DMARQ	82 ohm	22 ohm
INTRQ	82 ohm	22 ohm
IORDY (DDMARDY#, DSTROBE)	82 ohm	22 ohm
RESET#	33 ohm	82 ohm

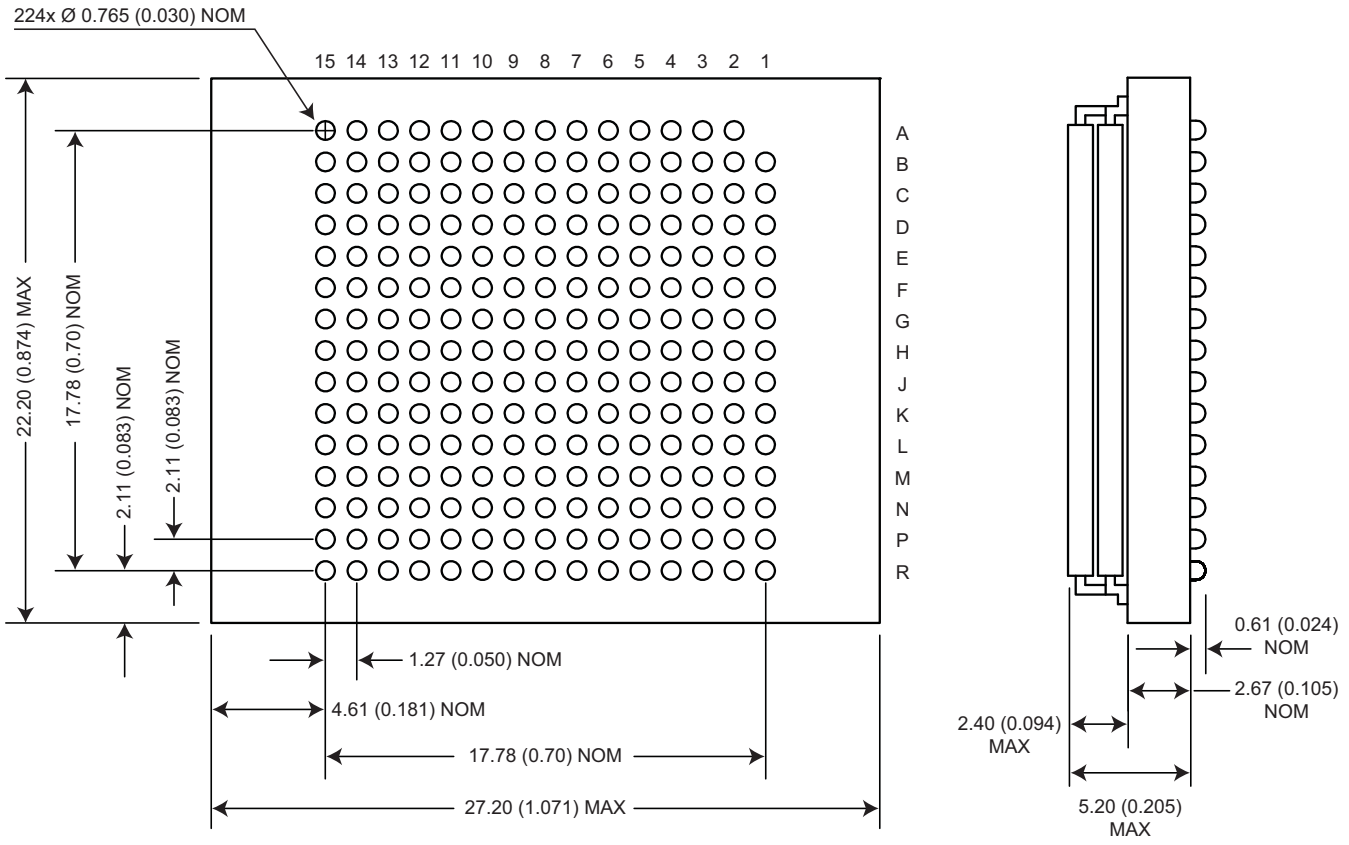
Note: Host Interface Terminator Resistors are at the discretion of the user, but are required for all Ultra DMA modes according to the ATA/ATAPI-6 Specification and the CFA CompactFlash Specification 4.1. Only those signals needing termination are listed in this table. If a signal is not listed, series termination is not needed for operation in an Ultra DMA mode. The actual termination values should be selected to compensate for transceiver and trace impedance to match the characteristic cable or board trace impedance.

PACKAGE DIMENSIONSFOR 4GB AND 8GB



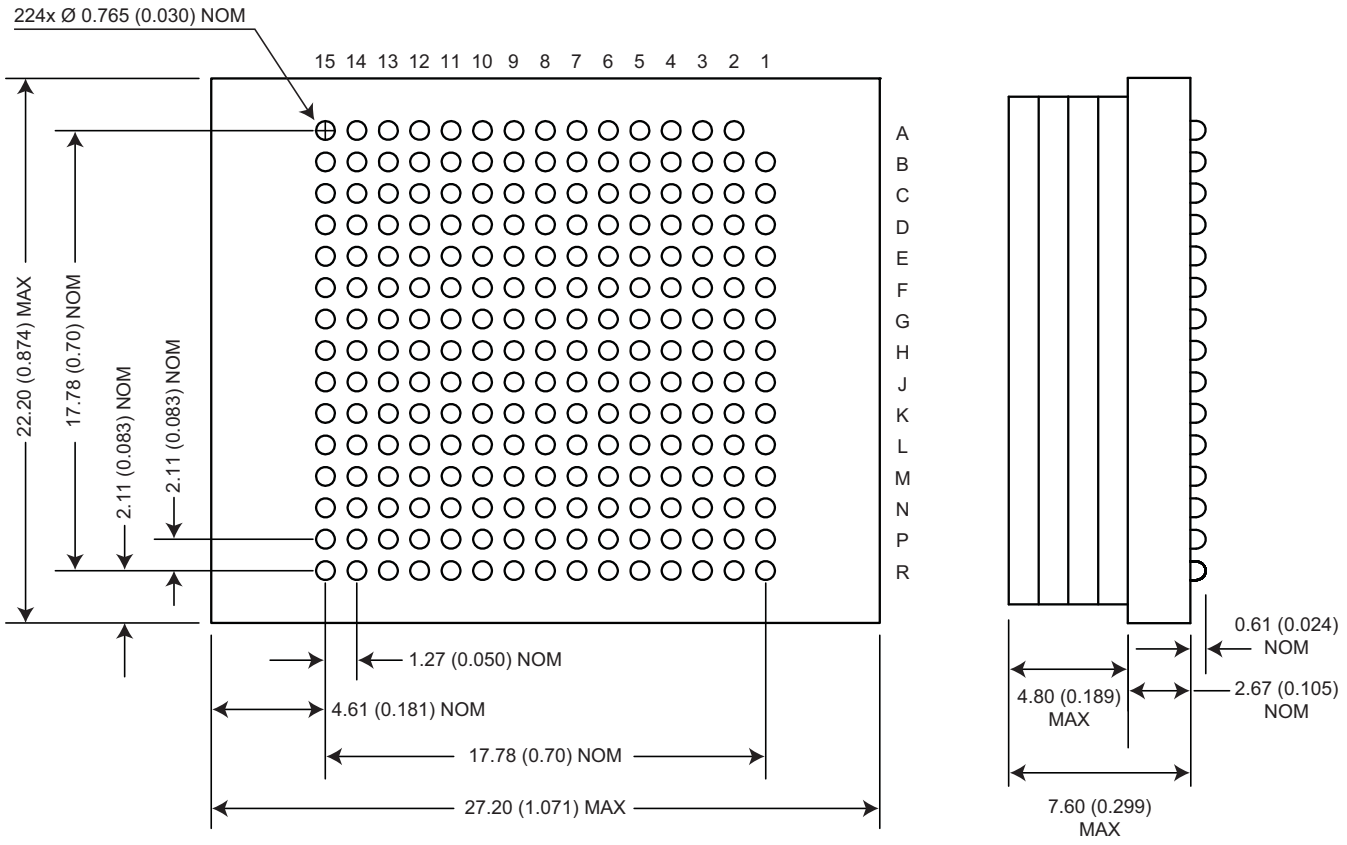
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE DIMENSIONSFOR 16GB



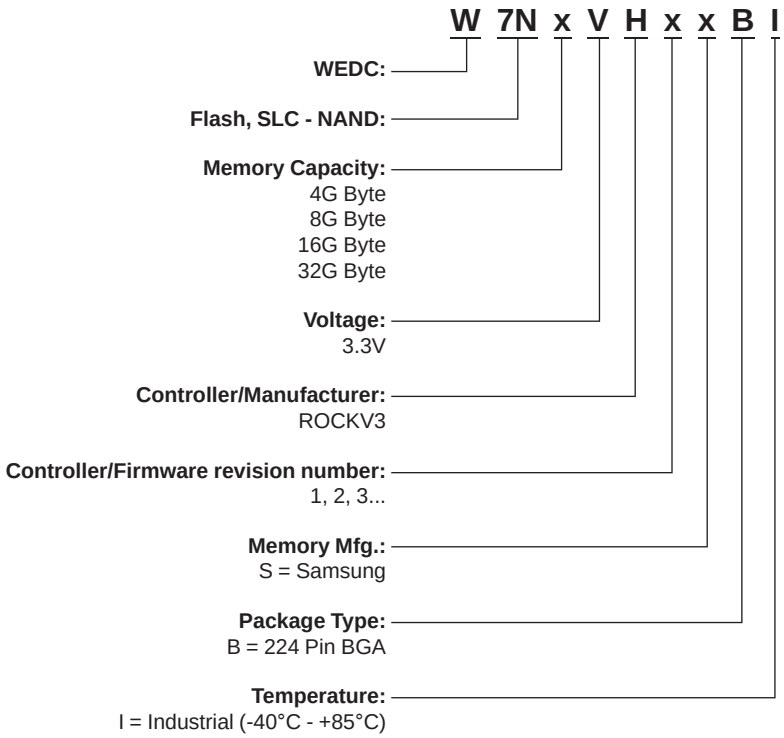
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE DIMENSIONSFOR 32GB



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

Part Numbering Guide



* For help selecting the proper and most current part number for your application please contact your local sales representative.

Example:

Part number for 4GByte: W7N4GVH1SBI

Document Title

SLC NAND SSD PBGA

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	May 2010	Initial
Rev 1	Changes (Pg. 1, 10) 1.1 Changed data sheet from initial to avanced 1.2 Updated MO drawings for the 4, 8, 16 and 32GB SSD's	July 2010	Advanced